MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

SECT
GENERAL DI

1.1 ORGANIZATION OF DATA SHEET

This document is composed of 4 section
MC145537EVK ADPCM Codec Evaluation
board and a list of key features. Section 2
functional block of the MC145537EVK and
describes the stand alone hardware opera
jumper positioning for this mode. It also disc
operation using two MC145537EVKs or on
Section 4 describes the software interface f
commands available via the on-board MC68

NO
This User's Manual - MC1
Evaluation Kit, corresponds
Circuit Board REVISION C (XI

1.2 INTRODUCTION

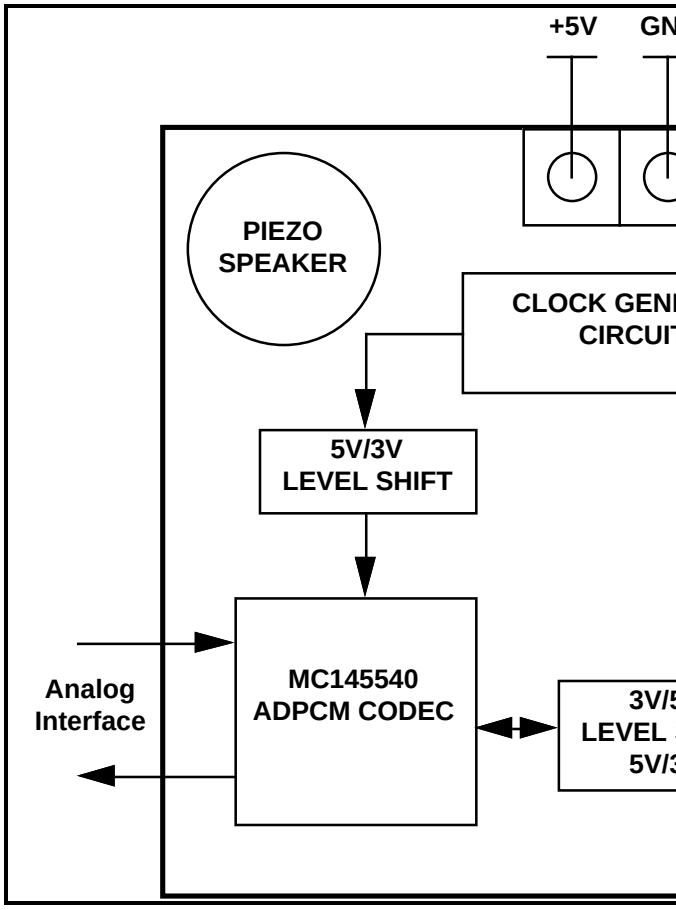
The MC145537EVK is the primary tool
MC145540 ADPCM Codec. The MC145537
hardware and software interface needed to
modes of the MC145540 ADPCM Codec.

Figure 1-1 on the following page is a funct
The MC145537EVK is comprised of the MC
from 2.7 to 5.25 volts, the 5 volt circuitry tha
MC68HC705C8P microcontroller and the I
level shifters which interface the ADPC
microcontroller.

User I/O to the board is provided via a numb
analog interfaces for the device: an industry
provided to connect the included handset,
transmit analog input, the BNC connector (
the wire clamp connector (P5) for access
speaker which is jumper selectable to be dri
digital interfaces including the DB25 conne
the computer terminal, a 2x20 pin header (P

Advance Information

MC145540 ADPCM C
EVALUATION KIT



This document contains information on a new product. Specifications an

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SECT
HARDWAR

NO

Please refer to the MC145537
of the hardware.

2.1 POWER SUPPLY CONFIGURATIONS

The MC145537EVK is powered by the three
at the top of the circuit board. This evaluatio
clock generator, microcontroller and EIA23
be powered by this 5 volt supply as selected
2.7 volts to 5.25 volts that is applied at the th

The MC145540 powers-up from a hardwa
charge pump running. This allows the devic
2.7 volts to as high as 5.25 volts. For 5 volt
position. This selects the 5 volt power sup
VEXT pin of the MC145540. The charge pur

For lower voltage applications (i.e. 3 volts
position, and jumper J1 should be in t
configuration connects the MC145540 VEX
the third terminal of P7 so that the MC1455
voltage power supply.

Jumper J12 allows the MC145540 to be co
or the lower voltage supply (VDD). This j
except to insert an ammeter for measuring th

Jumper J13 connects the MC145540 VD
applications with the charge pump turned off

2.2 CLOCK GENERATION CIRCUITRY

A 20.48 MHz crystal oscillator is used as
From this 20.48 MHz crystal, Frame Sync
Processor Clock (SPC) are derived for use b

the controlling clocks, and a 2x16 header
signals.

The MC145537EVK is powered by the three
at the top of the circuit board. This evaluatio
clock generator, microcontroller and EIA23
be powered by this 5 volt supply as selected
2.7 volts to 5.25 volts that is also applied at

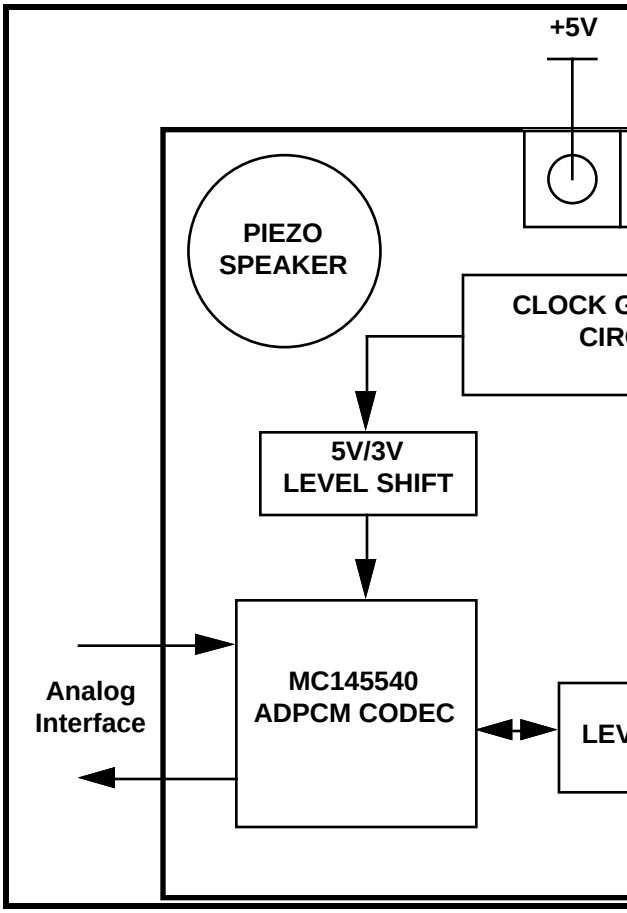

Figure 1-1. MC145537EVK

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1.3 FEATURES

GENERAL

- Provides Stand Alone Evaluat
- The kit provides analog to anal
  32 kbps ADPCM, 24 kbps ADF
  Motorola proprietary 16 kbps A
  ADPCM, 24 kbps ADPCM, CC
  proprietary 16 kbps ADPCM) t
- +5 Volt Only Power Supply or
- Easily Interfaced to Test Equip
  MC145537EVK or MC145536E
  Duplex Operation.
- Convenient Access to Key Sig
- Piezo Loud Speaker
- EIA232 Serial Computer Termi
  ADPCM Codec Features.
- Compatible Handset Provided
- Schematics, Data Sheets, and

MC145540 Features

- Single 2.7 to 5.25 Volt Power S
- Typical 3 Volt Power Dissipatic
- Differential Analog Circuit Desi
- Complete Mu-Law and A-Law
- Conforms to CCITT and ANSI
  32, 24 and 16 kbps data rates
- Universal Programmable Dual
- Programmable Transmit Gain,

MC145540 Features (cont.)

- Low Noise, High Gain, Three T
  Interface
- Push-Pull 300Ω Power Drivers
  Interface
- Push-Pull 300Ω Auxiliary Outp
- Voltage Regulated Charge Pur
  Voltage Applications
- Receive Side Noise Burst Dete
- Custom DSP Engine Optimize

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2.4 MC68HC705C8P

The MC68HC705C8P is one of Motorola's Serial Peripheral Interface port (SPI) MC145537EVK utilizes the SPI port for inte (SCP). The asynchronous interface is used computer terminal interface. The microco supports sixteen commands for prograr MC145540 ADPCM Codec.

The MC145537EVK is designed to acco currently supported by the resident software and D7), the push button switch (S1) and th MC145540 reset pin, the MCU reset pin, SC

FSYNC - Frame Synchronization Pulse

Frame Sync (FSYNC) is the 8 kHz signa (PCM) words. The ADPCM transcoding rate controlled by the width of the frame sync me pins respectively. The FST and FSR signals ADPCM Codec to determine the sample r analog conversions. FSYNC is presented to the MC145540 for FSR pin and FST pin resp

DSW1 allows the user to select the "width cycles. The individual switches of DSW1 resistors that are connected to the inputs o The value of DSW1 is loaded into the shift r BCLK signal. The inputs of this shift r microcontroller using the FW (Frame syn section 3 for the software command set. N be in the open position and that the microc open to this node for the clock circuit to oper

Figure 2-1 below indicates the proper dip s and 16 kbps long frame clocking, and 32 k For 64 kbps operation, switches 1, 2 and 3 output of the shift register has only one ris load / shift cycle. Refer to the MC145540 Da

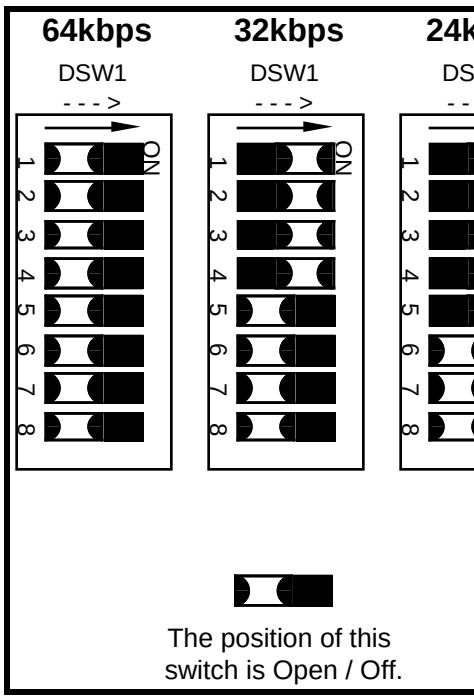

Figure 2-1. DSW1 Setting

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BCLK - ADPCM/PCM Data Bit Clock

Bit Clock (BCLK) is the Clock that controls
signal is presented to J6-B and J6-C for sel
for bit clock receive (BCLKR) and for bit cloc

P1 allows the user to select the frequency c
are 2.048 MHz, 1.024 MHz, 512 kHz, 256 k
note that only one frequency should be s
FSYNC signal is controlled by the BCLK cl
always 8 kHz when either of the BCLK frequ

256kHz

256 kHz is presented to J6-A for conne
sequencing clock for the codec-filter and
option for using BCLKR as the source for t
be programed via the SCP port at byte regis

SPC - Signal Processing Clock

SPC is a 20.48 MHz clock signal presente
(SPC, 21) pin for use as its digital signal pr
the SPC which are controlled by jumpers J1
should not be selected when J18 is selecte
the evaluation board at the same time. J1
drive the SPC pin of the MC145540. J8 sele
P9 header. This allows the on-board oscillat
the SPC pin of the MC145540 to the P9 he
drive the MC145540. If an off-board clock is
be removed from the board.

To use two MC145537EVK boards togethe
and J18 are removed from the boards. This
MC145536EVK which has the MC145480
ADPCM Transcoder. When two MC145537
ribbon cable that is about 2 inches (about 5
used for both evaluation boards. The jumpe
20.48 MHz clock may feed-through to the c
noise, which may be eliminated by externall
board to the other side of R3 of the other bo

2.3 MC145540 ADPCM CODEC

The MC145540 ADPCM Codec is a single
and an ADPCM encoder/decoder and th
applications requiring the digitization and
device is designed to operate over a wide vo
is ideal for battery powered as well as A
ADPCM Codec also includes a serial co
registers that permit a microcomputer to exe

The ADPCM Codec is designed to m
requirements of CCITT Recommendation G
T1.303 and CCITT Recommendation G.72
16 kbps ADPCM standard, CCITT Recomm
PCM conformance specification of the CCIT

Please refer to the included data sheet f
ADPCM Codec.

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J10	Invert TX and RX circuits to / fr operation
J11	Forces the microcontroller into
J12	Connects the VEXT pin of the independent of the level shifter accommodates current measu should usually be connected to
J13	Connects the MC145540 pin V used only when the MC14554(pump must be disabled by prog zero, bit 2.
J14	Connects either RO or PO- as connecter P4
J15A,B	J15A connects the AXO- signa connects the AXO- signal to th
J16	This jumper is a control input t microcontroller that two MC14 the 32 pin header connecter P both MC145540 ADPCM Code one computer terminal. This op microcontroller software. The u software development.
J17	Connects the level shifted 3 vo MC145540 SPC pin and to the be removed if the SPC pin is to
J18	Connects the SPC pin of the M P9. This jumper must be remov

2.5 MC145407 and EIA232 PORT DESCRI

The MC145407 is a single 5 volt power sup receivers in addition to an on-chip voltage develops the drive voltages to satisfy the I the level shifting and signal conditioning to produce an EIA-232 serial port which operat controlled by the microcontroller's crystal.

MC145540 configuration and control da MC145537EVK via a computer terminal. An connector (board side) and the appropriat serial computer interface is the 3 wire mini data, receive data and signal ground. Only connected. Upon turning on the board, or p message should appear on the screen:

Motorola MC145537EVK Evaluation KI MC145540>

Where X.X represents the software revision

If the computer terminal is configured correc the MCU reset switch is released, then the t the DB-25 connecter) may need to be exch This may be done by jumpers J10-A, J10- two jumper configuration options.

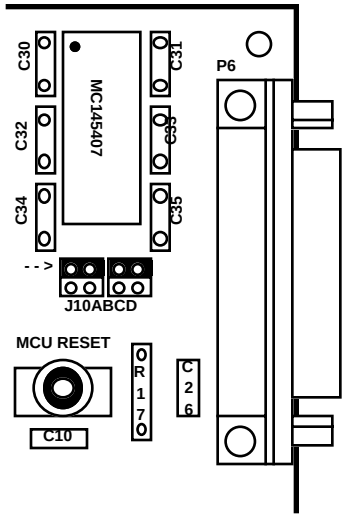

Figure 2-2. Jumper Positions for Switch EIA-232 Serial Compu

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2.6 COMPUTER TERMINAL INTERFACE D

The serial computer terminal interface uses
ground. These signals are on circuits 2, 3 a
MC145407 and EIA-232 port for reconfigu
computer terminal should be configured for:

1. 9600 bps (bits per second or 9600
2. Full-duplex
3. 8-Bit data words
4. 1 stop bit
5. Parity should be turned off
6. Linefeed automatic with return

2.7 JUMPER DESCRIPTIONS

The following table shows all on-board jum
Please reference the schematic for additiona

Jumper	Functionality
J1	If VDD is selected for 3 volts by +3 volt power supply input of P from the 5 volt supply.
J2	Sets VDD power supply of the power supply wire clamp conn for the logic level shifters and t
J3	Connects the on-board 20.48 M generate the 8 kHz FST, bit clo allows these clocks to be deriv
J4	Connects the on-board 20.48 M logic level shifter for driving the MC145540. This jumper allows oscillator to clock the SPC pin
J5A,B	Connects the 8 kHz FSYNC or respectively of the MC145540.
J6A,B,C	J6A connects the on-board 256 MC145540 for use as the inter pin as the input for an external be selected by programming th and J6C connect the on-board
J7A,B	Connects the on-board 256 kH 40 pin header connecter, P9. T PCM Codec-Filter on an MC14 MCLK function is similar to the of the MC145540.
J8	Connects a buffered on-board pin header connecter, P9 for o connected if Jumper J18 is con SPC pins of P9.
J9	Connects the ADPCM / PCM c ADPCM / PCM input (DR pin) operation.

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3.2 MC145537EVK to MC145537EVK Fu

The MC145537EVK evaluation boards were
header connecter with a ribbon cable, 36 inc
makes the necessary electrical connections
to-handset" path to be established. The thre
cable and therefore the MC145537EVK shou
compatibility with maximum digital noise imn
Codecs.

NO

Power (5 volt) and Grou
MC145537EVK to the seco
connect a second powe
MC145537EVK!

2.8 HANDSET

The compatible handset included with th
W3-K-EM-80, reverse polarity. The hands
connector. The handset incorporates a lo
receiver equipped with a hearing aid coil and

TRANSMITTER

Transmit Output Level @ 1000 Hz: -46 dBV

Output Impedance @ 100 Hz: 1000 ± 300Ω

RECEIVER

Receive Output Level @ 1000 Hz: 79 dBSPL

Receive Input Impedance @ 100 Hz: 150 Ω

For more detailed characteristics of the W3
Equipment Corporation in North America at

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SECT
OPERATING

The following information describes the
MC145537EVK may operate. There are ma
been described in this document that the
yourself with the included schematic dia
configuration that may prove beneficial for
there are specific questions on a particular
hesitate to contact your local Motorola Repre

3.1 MC145537EVK SINGLE BOARD AN

The following table shows all on-board jum
digital loopback which accommodates analo

Jumper	Position	
J1	3EXT	
J2	5V	
J3	CLK GEN	IN
J4	SPC	IN
J5A	FSYNC>FSR	IN
J5B	FSYNC>FST	IN
J6A	256k>BCLKR	OUT
J6B	BCLK>BLKCR	IN
J6C	BCLK>BCLKT	IN
J7A	BCLK>MCLK	OUT
J7B	256k>MCLK	OUT
J8	SPC>P6	OUT
J9	DT>DR	IN
J10	TOP ROW	
J11	MCU RES	OUT
J12	VDD	
J13	VDDA	OUT
J14	RO	
J15A	AXO>P5	OUT
J15B	AXO>SP1	IN
J16	BACK TO BACK	OUT
J17	SPC CLK	IN
J18	SPC OFF	OUT
P1	2048	

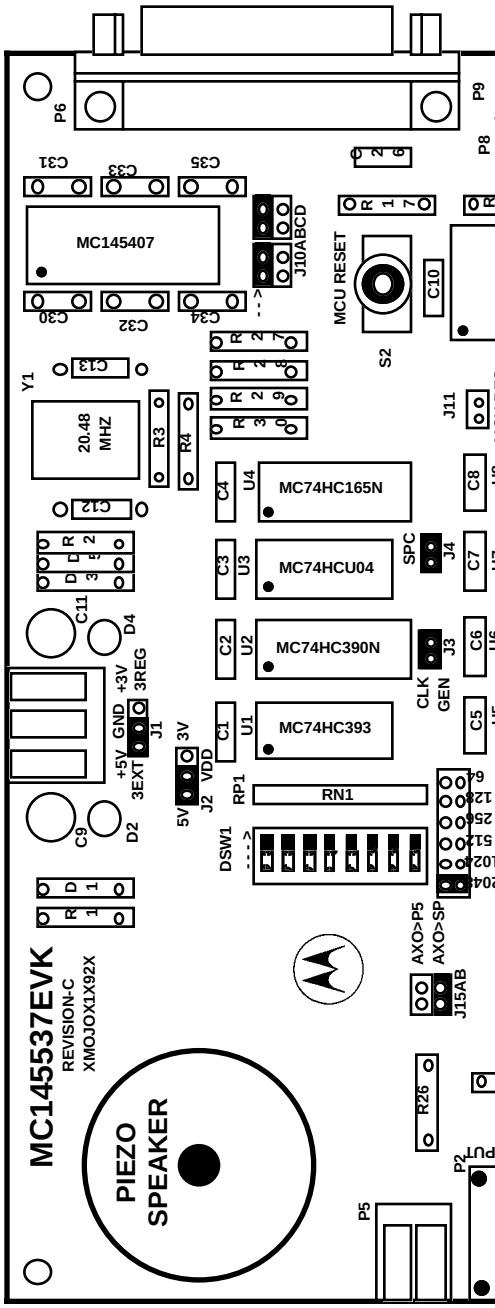

Figure 3-1. Jumper Settings for Digital L

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3.3 MC145537EVK to MC145536EVK Fu

The MC145536EVK and MC145537EVK ev
back-to-back. A 2x20 header connecter wi
length, makes the necessary electrical con
"handset-to-handset" path to be establish
noise in the grounds between these board
audio channel. To eliminate this noise, use a
the crystal on the MC145537EVK to one te
This will synchronize the two crystals and e
not present when a 36 inch (about one me
20.48 MHz oscillator is used for the SPC c
must be operated at 5 volts for logic level co
Codec and the MC145532 ADPCM Transco

NO

Power and Ground are busse
the MC145536EVK. Do not c
to the MC145536EVK!

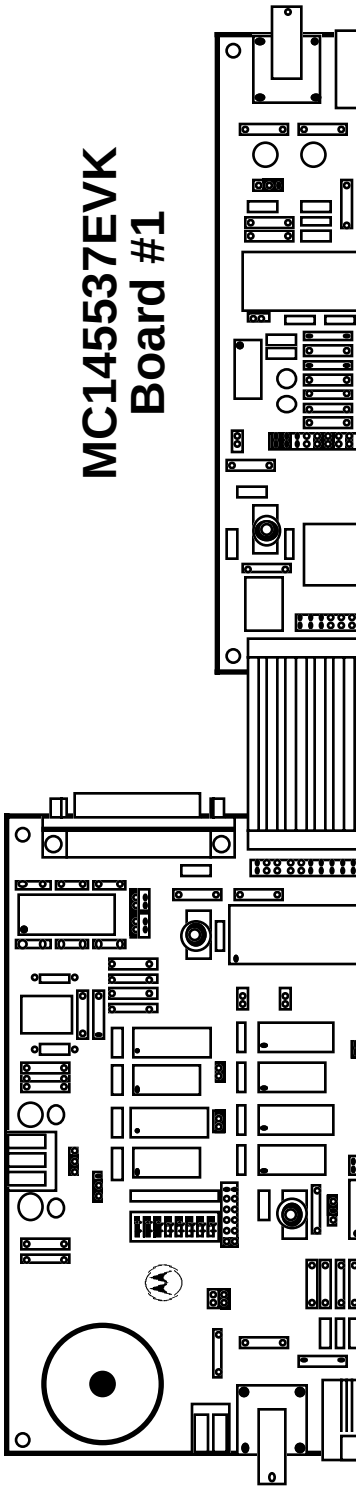

Figure 3-2. Recommended Cabling
Oper

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The following table shows all on-board jum
connecting one MC145537EVK to a secc
operation.

Jumper Configuration for first (clock generat

Jumper	Position	
J1	3EXT	
J2	5V	
J3	CLK	IN
J4	SPC	IN
J5	FSYNC>FSR	IN
	FSYNC>FST	IN
J6	256>BCLKR	OUT
	BCLK>BLKCR	IN
	BCLK>BCLKT	IN
J7	BCLK>MCLK	OUT
	256>MCLK	OUT
J8	SPC>P6	OUT
J9	DT>DR	OUT
J10	TOP ROW	
J11	MCU RES	OUT
J12	VDD	
J13	VDDA	OUT
J14	RO	
J15	AXO>P5	OUT
	AXO>SP1	IN
J16	BACK TO BACK	OUT
J17	SPC CLK	IN
J18	SPC OFF	OUT
P1	2048	

Jumper Configuration for second (clock rece

Jumper	Position	
J1	3EXT	
J2	5V	
J3	CLK	IN
J4	SPC	IN
J5	FSYNC>FSR	OUT
	FSYNC>FST	OUT
J6	256>BCLKR	OUT
	BCLK>BLKCR	OUT
	BCLK>BCLKT	OUT
J7	BCLK>MCLK	OUT
	256>MCLK	OUT
J8	SPC>P6	OUT
J9	DT>DR	OUT
J10	TOP ROW	
J11	MCU RES	OUT
J12	VDD	
J13	VDDA	OUT
J14	RO	
J15	AXO>P5	OUT
	AXO>SP1	IN
J16	BACK TO BACK	OUT
J17	SPC CLK	IN
J18	SPC OFF	OUT
P1	2048	

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SE
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4.1 COMPUTER TERMINAL SOFTWARE

The following is a list of all commands curre
their function. In all cases, an error in th
message on the CRT: `Error: unknow`
parameters specified is less than what the
`parameter(s) input` will be displayed o
routine expects all numbers and coefficients

HE (Help command)
Print out the command menu.

RE <logic state> (Reset command)
Force the reset line to the MC145540 to w
state. Recall that the reset line into the MC
held in the reset state when the logic state
reactivate cycle to occur,this command mu
reset pin low (RE 0), followed by a comma
This is an alternative to the reset pushbuttor

DR (Display all SCP registers)
Read all 10 SCP registers (plus silicon mas
on the computer terminal display.

SC [register address] <scp data> (SCP acce
Execute an access to SCP register specifiec
it is written to the register; otherwise, the a
the contents of the register after the access
terminal display. This command allows fu
display the status of byte register 2, (`SC 2`).
(`SC 2 40`). This command will also prograr
PO-, AXO+ and AXO- outputs to half of the
program all of the accessed byte register's fu

SS [register address] <scp data> (SCP acce
Same as the SC command explained abov
interface, whether for read or write. This is
necessary to synchronize some test equip
This successive read is terminated wh
microcontroller reset switch, S2 is depressed

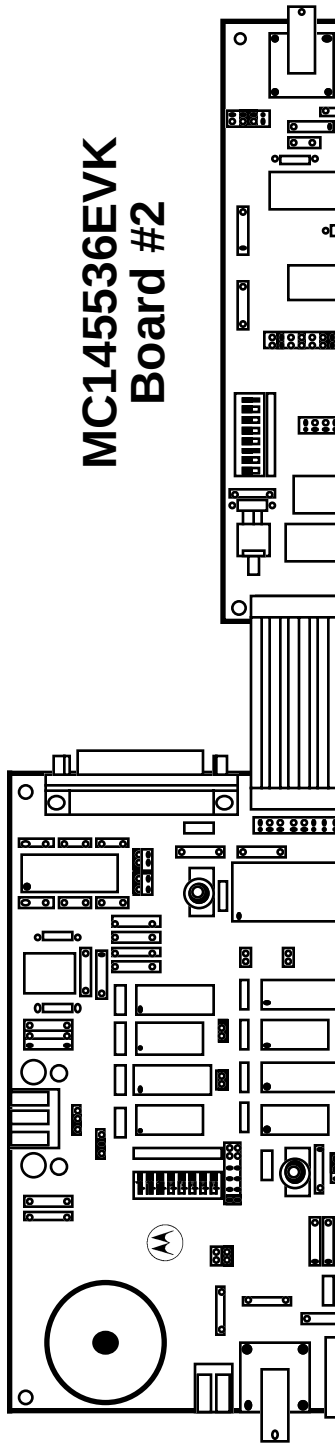

**Figure 3-3. Recommended Configurati
Oper**

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The following table shows all on-board jump
connecting an MC145537EVK to an MC145

MC145537EVK Jumper Configuration

Jumper	Position	
J1	3EXT	
J2	5V	
J3	CLK	IN
J4	SPC	IN
J5	FSYNC>FSR	IN
	FSYNC>FST	IN
J6	256>BCLKR	OUT
	BCLK>BLKCR	IN
	BCLK>BCLKT	IN
J7	BCLK>MCLK	OUT
	256>MCLK	OUT
J8	SPC>P6	OUT
J9	DT>DR	OUT
J10	TOP ROW	
J11	MCU RES	OUT
J12	VDD	
J13	VDDA	OUT
J14	RO	
J15	AXO>P5	OUT
	AXO>SP1	IN
J16	BACK TO BACK	OUT
J17	SPC CLK	IN
J18	SPC OFF	OUT
P1	2048	

MC145536EVK Jumper Configuration

Jumper	Position
J1	OUT
J2A	OUT
J2B	IN
J3A	OUT
J3B	IN
*J4	OUT
J5	OUT
J6	OUT
J7	IN
J8	IN
*J9	OUT
*J10	OUT
J11A	IN
J11B	OUT
J12A	IN
J12B	OUT
J13A	IN
J13B	OUT
J14A	OUT
J14B	IN
J15A	IN
J15B	OUT
J16	IN
J17	IN
J18	IN
J19	IN
J20	OUT
P1	2048
S1	ALL SWITCHES OPEN / CLO

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ME [memory address] <memory data> (Mem
Access the memory location specified by m
microcontroller operates in internal memor
goes from 0 to HEX 1FFF. If the address sp
and a memory data field has been inclu
location, otherwise the memory location is r
memory location after the access has been c

TG [coefficient] [attenuation] [tone generator
Program the tone generation function of the
field, with the coefficient and attenuation i
debugging aide, all SCP accesses required
displayed on the screen. e.g. TG 100 200
generator to a frequency of 697 hertz at an
amplitude would be (`TG 6D5 200 1`). Th
sequence of SC commands:

```
SC 7                 'REM Read BR7
(SC 7) OR HEX 08     'REM Logical OR
                     'REM Let BR7=H
SC 7 08              'REM Write HEX
SC 4 D5              'REM Write lower
SC 5 06              'REM Write to ton
                     'REM write the m
                     'REM coefficient
SC 7                 'REM Read BR7.
Is (SC 7) < HEX 80   'REM Check that
                     'REM read BR4 a
SC 4 00              'REM Write the le
                     'REM coefficient
SC 5 42              'REM Write to ton
                     'REM write the m
                     'REM coefficient
SC 7                 'REM Read BR7.
Is (SC 7) < HEX 80   'REM Check that
                     'REM read BR4 a
SC 7 0A              'REM Turn on ton
```

MA <encoding mode> (Encoding law comma
If an encoding mode field is specified, set th
or A-law encoding (encoding mode = 1). C
used.

E2 [256 kHz clock option] (External 256 kHz
Set or reset the external 256 kHz clock op
clock option parameter: 1 to set the option, 0

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IO <I/O mode>
Set or display the I/O mode of the part, repr
This command allows easy access to the f
below summarises these modes. Pleas
information.

I/O Mode(1:0)
00
01
10
11

Figure 4-1. Input / Output Modes of the M

CD <Charge pump option>
Set or reset the charge pump disable optior
the operation of the charge pump; CD 1 will

ST <Sidetone Gain>
Set or display the gain factor to be applied t
of the Codec section of the part to the samp
Codec. Numbers in the range of 0 to 7 are e

XG <Transmit Gain>
Set or display the gain factor to be applied t
transmit filter. Numbers in the range of 0 to 7

AG <Analog Receive Gain>
Set or display the gain factor to be applied t
receive filter of the Codec section of the
expected.

DG <Digital Receive Gain>
Set or display the gain factor to be appli
processed by the decoder function in the
HEX 7F are expected.

FW [Frame sync pulse width]
The width of the sync pulse to be applied to
switch DSW1, or by the on-board microcor
access to the input of the parallel loaded s

status of the DSW1 and if any of DSW1's s
not try to drive the shift register. If the paran
microcontroller will not try to program the s
open the clock circuit will generate an FSYN
The microcontroller may be used to shorte
the value of the FW parameter to other than
load that parameter into the shift register,
closed. The value of Frame sync pulse wi
HEX 80 to HEX FF, or else the number 0. A
kbps; HEX F0 puts the board into 32 kbps;
C0 puts the board into 16 kbps; HEX 80 puts

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